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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AGGARWAL, YOGESH K	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 01/05/2005

11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/680,239	PAIN ET AL.	
	Examiner	Art Unit	
	Yogesh K Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-15* is/are allowed.

6)☒ Claim(s) *1,2,7-11,16,17 and 19* is/are rejected.

7)☒ Claim(s) *3-6,18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments, see amendment (Paper No. 9), filed 07/29/2004, with respect to the rejection(s)of claim(s) 1-19 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Zhou et al. (US Patent # 6,787,749).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 7-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhou et al. (US Patent # 6,787,749).

[Claim 1]

Zhou et al. teach a photo-sensing array (figure 1, element 110) of a plurality of sensing pixels (210) arranged in rows and columns, each pixel having a photo-sensing element (211) to produce charge in response to incident photons from an object and an in-pixel circuit (213) to convert said charge into an electrical pixel signal representing said charge (col. 4 lines 61-67) and an integrator array (130) of a plurality of integrators (231) arranged in rows and columns respectively equal to said rows and columns of said photo-sensing array, wherein integrators of each column are coupled to receive electrical pixel signals from only one designated column of

sensing pixels in said photo-sensing array and are operable to produce time-delayed integration signals representing the object (col. 3 lines 44-51) after each sensing pixel is sampled and read out for a number of times equal to a number of said rows in said photo-sensing array (col. 8 lines 45-61).

[Claim 2]

Zhou et al. teaches a combination of capacitor (231) and transistor (232) is read as capacitor-switched integrator.

[Claim 7]

Zhou et al. teaches that the APS circuit having an amplifier (col. 1 lines 31-37).

[Claim 8]

Zhou et al. teaches that the APS circuit has a photo-gate (col. 4 lines 65-66).

[Claim 9]

Figure 3c discloses an equivalent reset circuit for all APS pixels (col. 6 lines 1-10).

[Claim 10]

Official Notice is taken of the fact that it is very well known in the art to have at least one ADC being used to digitize one output from an integrator array in order to edit the image digitally.

[Claim 11]

Zhou et al. teach that the APS pixel being consecutively sampled reset level and the signal level by the buffer 220 (col. 5 lines 8-13).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 16, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (US Patent # 5,917,620) in view of Antonelli et al. (US Patent # 6,259,108).

[Claim 16]

Hasegawa et al. teach a method comprising using a linear sensing array of pixels (col. 2 lines 65-67, figure 6, element 1701-1703). In a scanner it is very well known in the art that there is a relative direction of movement between the object and the sensors, coupling a linear integrator array (1710, 1712) of integrators sensing array to sample object generated by multiple frames sensing array (col. 3 lines 12-21) and images of the spatially shifting the mapping from the sensing frames along the predetermined direction to produce a summed signal that sums pixel signals from different pixel locations different frames corresponding common image from a location on object (col. 2 lines 56-64) except that each pixel internally converts radiation-induced charge into an electrical pixel signal. However Antonelli teaches a linear array sensor with a single linear array, or two or more parallel rows of light sensing pixels, may use CCD (charge coupled device) pixels, or may use CMOS (complementary metal oxide semiconductor) APS (active pixel sensing) pixels, photo-diode pixels, or any other linear array of light sensing technology (col. 4 lines 17-24). Therefore taking the combined teachings of Hasegawa and Antonelli, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have an in-pixel circuit internally converting radiation-induced charge into an electrical pixel signal (a typical feature of APS pixels) into the CCD structure of Hasegawa wherein CCD and APS are obvious variations of each other as taught by Antonelli.

[Claim 17]

Official Notice is taken of the fact that it is notoriously common to sample twice the reset and signal levels (CDS) of a pixel during a frame in order to reduce noise.

[Claim 19]

See Claim 2.

Allowable Subject Matter

6. Claims 12-15 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to suggest or show fairly an integrator array fabricated on a second area of said substrate adjacent first area, said integrator array having m amplifiers electrically coupled to said m columns active pixel sensors, respectively, wherein each amplifier is coupled n pairs capacitors so that each pair different active pixel sensors in a respective column that are generated at different times produce a summed signal.

8. Claims 3-6, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. As for claims 3 and 18, the prior art fails to suggest or show fairly an operation of one integrator on a signal from one sensing pixel is temporarily overlapped with another operation of an adjacent integrator on another signal from a respective adjacent sensing pixel.

10. As for claim 4, the prior art fails to suggest or show fairly wherein a single terminal of said capacitor-switched integrator first sampling coupled from a capacitor that stores a first signal first sensing pixel and second sampling capacitor a second signal from second sensing

pixel adjacent said first sensing pixel, said first and second signals being generated at different times.

11. As for claim 5, the prior art fails to suggest or show fairly wherein said capacitor-switched integrator is a differential integrator which has first input terminal to receive an electrical pixel signal and second input terminal to receive a reference signal.

12. As for claim 6, the prior art fails to suggest or show fairly wherein capacitor-switched integrator includes a single-ended amplifier whose coupled circuit having a reset sampling capacitor, said reset switches positioned sampling capacitor and said integrating capacitor, plurality of circuit connect integrating capacitor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (703) 305-0346. The examiner can normally be reached on M-F 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
December 22, 2004

ANDREW CHRISTENSEN
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